WHAT IS CLAIMED IS:

1. A method for exposing a layer with a light comprising:

disposing a mask including a pattern shape over the layer formed on a substrate; and

scanning the mask with the light, such that a direction of the scanning is substantially perpendicular to a longitudinal direction of the pattern shape to form a pattern.

2. The method of claim 1, wherein the pattern formed on the substrate is electrically coupled with a conductive pattern disposed in a different layer from the pattern to generate a coupling capacitance, wherein an insulation layer is disposed between the pattern and the conductive pattern.

3. The method of claim 1, wherein the pattern formed on the substrate corresponds to a data line.

4. The method of claim 3, further comprising:

forming an insulation layer on the substrate having the data line; and

forming a pixel electrode as a conductive pattern on the substrate having the insulation layer, wherein a direction of scanning is substantially perpendicular to a longitudinal direction of the data line during an exposure process for forming the pixel electrode.

5. The method of claim 1, wherein the substrate has a size of more

than or equal to seventeen inches.

6. The method of claim 1, wherein the substrate corresponds to a substrate of a patterned vertical alignment mode liquid crystal display device having a size of nineteen inches.

7. The method of claim 4, wherein an interval between the data line and a pixel electrode formed on the substrate is at least 6.25 ㎛.

8. The method of claim 1, wherein one cell is exposed by the mask.

9. A method of forming a thin film transistor substrate for a liquid crystal display device comprising:

forming a gate wiring layer on a substrate;

etching the gate wiring layer to form a gate wiring that includes a gate line, a gate end and a gate electrode;

forming a gate insulation layer on the substrate having the gate wiring formed on the substrate;

forming a semiconductor layer pattern and an ohmic contact layer pattern on the gate insulation layer in sequence;

forming a data wiring layer on the substrate having the semiconductor layer pattern and the ohmic contact layer pattern;

forming a photoresist layer on the data wiring layer;

disposing a mask including a pattern shape over the photoresist layer formed on the substrate;

scanning the mask with a light, such that a direction of the scanning is substantially perpendicular to a longitudinal direction of the pattern shape to expose the photoresist layer;

patterning the data wiring layer to form a data wiring including a data line crossing the gate line, a data end connected to the data line, a source electrode connected to the data line, and a drain electrode in an opposite position to the source electrode around the gate electrode;

forming a protection layer on the substrate having the source and drain electrodes formed thereon;

patterning the gate insulation layer and the protection layer to form contact holes, the contact holes exposing the gate end, the data end and the drain electrode, respectively;

forming a transparent conductive layer; and

etching the transparent conductive layer to form an auxiliary gate end being electrically connected to the gate end, an auxiliary data end being electrically connected to the data end, and a pixel electrode being electrically connected to the drain electrode.

10. The method of claim 9, wherein a direction of scanning is substantially perpendicular to the longitudinal direction of the data line during an exposure process of a photoresist layer for forming the pixel electrode.

11. The method of claim 9, wherein an interval between the data line and the pixel electrode on the substrate is at least 6.25 ㎛.

12. The method of claim 9, wherein one cell is exposed by the mask.

13. The method of claim 9, wherein two cells are simultaneously exposed by the mask.

14. A method of manufacturing a thin film transistor substrate for a liquid crystal display device, comprising:

forming a gate wiring layer on a substrate;

etching the gate wiring layer to form a gate wiring that includes a gate line, a gate end and a gate electrode;

forming a gate insulation layer on the substrate having the gate wiring formed thereon;

forming a semiconductor layer, an ohmic contact layer and a conductive layer on the gate insulation layer in sequence;

forming a photosensitive layer pattern by scanning with a light through a mask, wherein a direction of scanning is substantially perpendicular to a longitudinal direction of a data line to be formed during an exposure process, and the photosensitive layer pattern includes a first portion, a second portion thicker than the first portion, and a third portion thinner than the first portion;

forming a data wiring including a data line, a data end connected to the data line, a source electrode and a drain electrode, an ohmic contact layer pattern and a semiconductor layer pattern using the photosensitive layer pattern as a mask;

forming a protection layer;

patterning the protection layer and the gate insulation layer to form contact holes, the contact holes respectively exposing the gate end, the data end and the

drain electrode;

forming a transparent conductive layer; and

etching the transparent conductive layer to form an auxiliary gate end, an auxiliary data end and a pixel electrode, the auxiliary gate end being connected to the gate end, the auxiliary data end being connected to the data end, the pixel electrode being connected to the drain electrode.

15. The method of claim 14, wherein a direction of scanning is substantially perpendicular to the longitudinal direction of the data line during an exposure process of a photoresist layer for forming the pixel electrode.

16. The method of claim 14, wherein an interval between the data line and the pixel electrode on the substrate is at least 6.25 ㎛.

17. The method of claim 14, wherein one cell is exposed by the mask.

18. The method of claim 14, wherein a plurality of cells are simultaneously exposed by the mask.

19. The method of claim 14, wherein the first portion is positioned between the source electrode and the drain electrode, and the second portion is positioned over an upper portion of the data wiring.